AMENDMENTS TO THE SPECIFICATION:

Please amend the following paragraphs of the published application as follows:

[0012] The parallel processor is preferably an array processor, such as a ~~SIMD~~ Single Instruction, Multiple Data (SIMD) processor. The parallel processor may further comprise means to serialise and/or synchronise multiple accesses/updates to said shared state.

[0039] The State Elements could be utilised in ~~MIMD~~ Multiple Instruction, Multiple Data (MIMD) architecture or, indeed, anywhere that there is a conflict to resolve. It is particularly applicable to SIMD architecture, however, because MIMD is more tolerant to indeterminism in memory access whereas SIMD prefers everything to be deterministic.

[0041] In preferred implementations, the command line allows commands to be issued to access and modify a piece of memory or deposit micro-code in the state element. The state element therefore consists of a basic memory plus an ~~ALU~~ Arithmetic Logic Unit (ALU), a controller unit where the microcode is written to, and special function units, such as addition units. Part of the design philosophy is to enable the element to become part of Applicant's toolkit, where required functions can be "bolted" on as necessary.